IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Doris, et al.

Serial No.:	10/710,272	**Group Art Unit:**	2895
Filed:	June 30, 2004	**Examiner:**	Tsai, H.
For:	METHOD AND STRUCTURE FOR STRAINED FINFET DEVICES		

Commissioner of Patents
Alexanderia, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL

Sir:

Appellants respectfully appeal the rejection of claims 1-4, 6, 10-15, and 23-30 in the Office Action dated December 14, 2009. A Notice of Appeal was timely filed on February 26, 2010.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6, 10-15, and 23-30 are all the claims presently pending in the application. Claims 5, 7-9, and 16-22 are canceled.

Claims 1-4, 6, 10-15, and 23-30, all claims currently pending, stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over US Patent Publication 2004/0173812 to Currie, et al., further in view of US Patent Publication 2004/0108559 to Sugii, et al., US Patent Publication 2005/0242395 to Chen et al.

The rejection for claims 1-4, 6, 10-15, and 23-30 is being appealed, in the format of the three issues identified below.

IV. STATUS OF AMENDMENTS

A Request for Reconsideration Under 37 CFR §1.116 was filed on February 16, 2010. In the Advisory Action mailed February 23, 2010, the Examiner indicated that the arguments in the Amendment Under 37 CFR §1.116 were not persuasive and that the rejection based on Currie was maintained.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellants' invention, as disclosed and as claimed in independent claim 1, is directed to a method of forming an electronic device, said method including forming at least one localized stressor region within the device.

As explained at lines 14-15 of page 4 of the disclosure, strained silicon is conventionally grown epitaxially as a layer on a SiGe layer structure, but, as explained at lines 8-10 of page 6, such strained silicon has been difficult to integrate in FinFET devices because of the geometry of the fin and gate and because of the fabrication process.

Therefore, Appellants have developed the concept of the present invention, wherein stressor regions are formed locally within the device. In the exemplary embodiment discussed in the disclosure, a FinFET device is used to demonstrate the process of incorporating a stressor region on specific components within the FinFET structure.

The locations within the specification and figures of the claimed invention for the independent claims and dependent claims being argued separately are as follows:

1. (Rejected) A method of forming an electronic device (Figures 3-8), said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins (301, Figure 6) interconnected by fin connectors (302, Figure 6), said method comprising:

forming at least one localized stressor region (601, Figure 6) within said device, said at least one localized stressor region being located on one of said fin connectors (302, Figure 6) as a region of stressor material filling in an interior portion of said fin connector (paragraphs 0033 and 0035]).

2. (Rejected) The method of claim 1, wherein said at least one localized stressor region comprises a first localized stressor region, said method further comprising:

forming a second localized stressor region within said device (302, Figure 6),

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed (Figures 9 and 10; paragraph [0040]).

6. (Rejected) The method of claim 2, wherein said first and second localized stressor regions are formed on said fin connectors of said FinFET as regions of stressor material filling in interior portions of respective two fin connectors (Figures 6 and 7; paragraphs [0033,0034]).

14. (Rejected) A method of forming a stress region in an electronic device (Figures 3-8), said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins (301, Figure 7) interconnected by fin connectors (302, Figure 7), said method comprising:

forming a first localized stressor region within said device on a first fin connector (302, Figure 7, left side of figure) as comprising a first region of stressor material filling in an interior portion of said first fin connector (701, Figure 7, left side of figure); and

forming a second localized stressor region within said device on a second fin connector as comprising a second region of stressor material filling in an interior portion of said second fin connector (701, Figure 7, right side of figure),

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed (see Figures 9 and 10; paragraph [0040]).

30. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to create an asymmetrically stressed region (paragraph [0050]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellants present the following issue for review by the Board of Patent Appeals and Interferences:

ISSUE #1: THE 35 U.S.C. § 103(a) REJECTION FOR INDEPENDENT CLAIM 1, BASED ON U.S. PATENT APPLICATION PUBLICATION 2004/0173812 TO CURRIE, ET AL., FURTHER IN VIEW OF US PATENT APPLICATION PUBLICATION 2004/0108559 TO SUGII, ET AL., OR US PATENT APPLICATION PUBLICATION 2005/0242395 TO CHEN ET AL;

ISSUE #2: THE 35 U.S.C. § 103(a) REJECTION FOR INDEPENDENT CLAIM 14 AND DEPENDENT CLAIM 6, BASED ON U.S. PATENT APPLICATION PUBLICATION 2004/0173812 TO CURRIE, ET AL., FURTHER IN VIEW OF US PATENT APPLICATION PUBLICATION 2004/0108559 TO SUGII, ET AL., OR US PATENT APPLICATION PUBLICATION 2005/0242395 TO CHEN ET AL; and

ISSUE #3: THE 35 U.S.C. § 103(a) REJECTION FOR DEPENDENT CLAIM 30, BASED ON U.S. PATENT APPLICATION PUBLICATION 2004/0173812 TO CURRIE, ET AL., FURTHER IN VIEW OF US PATENT APPLICATION PUBLICATION 2004/0108559 TO SUGII, ET AL., OR US PATENT APPLICATION PUBLICATION 2005/0242395 TO CHEN ET AL.

VII. ARGUMENTS

ISSUE #1: THE REJECTION FOR INDEPENDENT CLAIM 1, AS BASED ON CURRIE, FURTHER IN VIEW OF EITHER SUGII OR CHEN

In summary, Appellants respectfully submit that the prior art rejection of record fails to demonstrate all elements of the claimed invention, since there is no demonstration of providing a localized stressor on the fin connectors of a finFET as a filled-in region on the interior portion of the finFET fin connectors.

Appellants are unable to find any reasonable support in either previously-cited Currie or Sugii or Chen, to form a localized stressor within the interior region of a fin connector of a FinFET, as required by the plain meaning of the claim language. Indeed, if anything, the references currently of record clearly demonstrate that there are many alternative ways to provide stressors in different types of devices. Rather, at most, primary reference Currie provides localized stressors in source/drain regions.

Therefore, to begin with, Appellants respectfully traverse the Examiner's findings of facts, as follows:

1. The Examiner points to regions 144,148 within primary reference Currie as allegedly demonstrating a localized stressor region of stressor material filling in an interior portion of a fin connector of a FinFET, further pointing to Figures 10D-10E and paragraphs [0016 and 0077] of Currie.

In response, Appellants respectfully submits that region 144, 148 is clearly defined in the second and third sentences of paragraph [0077] as recesses located in the source and drain regions 102,104, not a fin connector of a FinFET:

"*For example, first and second recesses 144, 148 may be defined in source region 102 and drain region 104 that include Si .... Recesses 144, 148 may be filled with a second material 150 with a lattice constant larger than that of Si, such as SiGe, thereby inducing compressive strain in channel region 108.*"

Therefore, Appellants respectfully expressly traverse the Examiner's finding of fact that Currie's paragraph [0077] teaches or suggests incorporating a localized stressor in a fin connector of a FinFET, let alone the interior portion of the fin connector.

Appellants are unable to find any suggestion in primary reference Currie to incorporate a localized stressor within the interior portion of a fin connector of a FinFET.

Appellants respectfully request that the Board find that the rejection of record errs in its characterization that primary reference Currie demonstrates a localized stressor located on the interior portion of a fin connector of a FinFET. Moreover, Appellants also respectfully request that the rejection of record also, therefore, fails to properly identify the differences between primary reference Currie and the claimed invention, thereby failing to provide the proper foundation for an obviousness rejection.

2. Appellants also respectfully request that the Board confirm that neither secondary reference Sugii nor secondary reference Chen teaches or suggests incorporating a localized stressor within the interior portion of a fin connector of a FinFET.

3. Appellants also respectfully request that the Board confirm that the Examiner fails to provide in the rejection of record any motivation whatsoever to move the stressor in primary reference Currie from the source/drain regions of a device to the fin connector region. Indeed, if anything, primary reference Currie would teach placing the localized stressors adjacent to the channel region rather than the more distal location on fin connectors 601 such as shown in Figure 6 of the present application.

That is, in Figure 8 of the present application, the source/drain regions are shown as regions 803,804 adjacent to the source/drain spacer 501 (see paragraph [0037]). According to the teachings of primary reference, the localized stressors would be placed in regions 803, 804 in a FinFET device, not in regions 302 as required by the independent claims.

4. That is, the Examiner fails to demonstrate any reference providing objective evidence that it was known in the art at the time of the present invention that primary reference Currie would be improved by relocating its localized stressor from the source/drain to a fin connector.

5. Nor does the Examiner provide any reference providing objective evidence that it was known in the art at the time of the present invention that incorporating a localized

stressor on the interior portion of a fin connector of a FinFET was known as a substitute for a localized stressor on a source/drain of a simple FET.

The most that can reasonably be deduced from the references of record is that FinFETs were known in the art at the time of the invention and that the claimed invention, therefore, would have been possible. Indeed, on page 7 of the latest Office Action, the Examiner clearly states that the standard being applied in the present evaluation is based on the conclusion that one of skill "would have recognized" that the claimed invention was possible:

"It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that localized stressor trench (recess) region can be formed on a fin connector as shown in fig. 28 of Sugii et al. or figs. 3-5 of Chen et al. because [a] fin connector connects source/drain regions of two FET transistors together."

However, such demonstration of mere possibility at the time of the invention is insufficient, since the correct standard for obviousness requires an articulation of a reasonable rationale to modify the primary reference to arrive at the claimed invention, and the rejection of record is based on the wrong standard for obviousness. A mere conclusory statement that one of skill would have "recognized that the claimed invention was possible at the time of the invention" is nothing but a rationale based on improper hindsight.

In the final two paragraphs of the Advisory Action mailed on February 23, 2010, the Examiner states:

"Since,[sic] Currie et al. teaches forming localized stressor regions (see fig. 10E, 11) within the device on the fin connector as comprising of stressor material filling in an interior portion of the fin connector can be applicable to transistors with multiple or wrap-around gates [sic]. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channel of which may be oriented horizontally or vertically), and Sugii et al., or Chen teaches a fin-FET having fin connectors, hence the combination of Currie and Sugii or Chen is proper.

Therefore, it is clearly[sic] that the combination of Currie and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international [sic] v Teleflex of "a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability".

And, it is also clearly [sic] that the combination of Currie and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international [sic]v. Teleflex of "if this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103."

In response, Appellants first again respectfully traverse the Examiner's characterization in the first sentence recited above from the Advisory Action that primary reference Currie teaches incorporation of a localized stressor on an interior portion of a fin connector of a FinFET, since Currie's Figures 10-11 are both demonstrating source/drains of a simple FET, not fin connectors of a FinFET, as would be required to satisfy independent claim 1.

Second, Appellants respectfully submit that the combination of Currie and Sugii or Chen, even if considered proper, would only result in placing the localized stressor region of Currie on the source/drain regions of all of the devices demonstrated in the cited references. As explained above, relative to the FinFET shown in Figure 8 of the present application, this means that the localized stressors of Currie would be placed in regions 803,804, not in the interior of fin connectors 302.

In contrast, the Examiner's initial burden in the obviousness rejection of the present evaluation is to provide a reasonable rationale to relocate the localized stressors of Currie to be on the interior portion of a fin connector of a FinFET, thereby resulting in the claimed invention. Merely demonstrating existence of FinFETs is insufficient to meet this burden. None of the references of record suggest that it was a known improvement or substitution to make the necessary modification to arrive at the invention described in claim 1.

In the configuration shown in Figure 8 of the present application, the Examiner's initial burden would be to provide a reasonable rationale to relocate localized stressors placed in source/drain regions 803, 804 (in accordance with the source/drain localized stressors of primary reference Currie) to be in fin connectors 302.

Relative to the Examiner's reliance upon the *KSR* holding, as recited above, Appellants respectfully submit that the references of record do not demonstrate that

relocating a localized stressor from a source or drain was known in the art at the time of the present invention to be a "predictable variation" or that it would be "obvious to try" the relocation necessary to arrive at the claimed invention. Without providing some objective evidence that the relocation of stressors from a source/drain to an interior portion of a fin connector, the Examiner's statements above are merely conclusory statements based on improper hindsight.

Indeed, the holding in KSR also states (emphasis by Appellants):

"*When it first established the requirement of demonstrating a teaching, suggestion, or motivation to combine known elements in order to show that the combination is obvious, the Court of Customs and Patent Appeals captured a helpful insight. See Application of Bergel, 292 F. 2d 955, 956–957 (1961). As is clear from cases such as Adams, a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.*"

Appellents have demonstrated that none of the references relied upon in the rejection of record demonstrates the element of the claimed invention of a localized stressor as an interior portion of a fin connector of a FinFET. Nor does the rejection of record even properly identify the differences between primary reference Currie and the claimed invention. Finally, Appellants submit that the rejection of record fails to provide a reasonable rationale to modify primary reference Currie to arrive at the invention defined in independent claim 1.

ISSUE #2: THE REJECTION FOR INDEPENDENT CLAIM 14 AND DEPENDENT CLAIM 6, AS BASED ON CURRIE, FURTHER IN VIEW OF EITHER SUGII OR CHEN

Appellants respectfully submit that the errors discussed above for ISSUE #1 apply equally to ISSUE #2. Additionally, this issue includes the failure of the rejection of record to provide motivation to relocate one of the two localized stressors of primary reference Currie from the source to be on one fin connector of a FinFET and to relocate the localized stressor from the drain to a second fin connector of the FinFET.

ISSUE #3: THE REJECTION FOR DEPENDENT CLAIM 30, AS BASED ON CURRIE, FURTHER IN VIEW OF EITHER SUGII OR CHEN

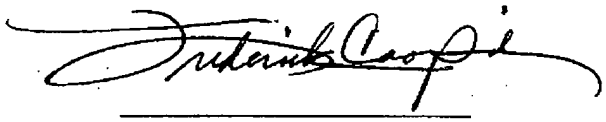
Appellants expressly traverse the Examiner's finding of fact that paragraph [0077] of primary reference Currie reasonably makes any suggestion of asymmetric stressing using localized stressors.

CONCLUSION

In view of the foregoing, Appellants submit that claims 1-4, 6, 10-15, and 23-30, all the claims presently rejected in the application, are clearly enabled and patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove the rejection of claims 1-4, 6, 10-15, and 23-30 based on Currie.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account number 09-0458.

Respectfully submitted,



Dated: April 24, 2010

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VIII. CLAIMS APPENDIX

Claims, as reflected upon entry of the Amendment Under 37 CFR §1.116 filed on October 27, 2008:

1. (Rejected) A method of forming an electronic device, said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors, said method comprising:

forming at least one localized stressor region within said device, said at least one localized stressor region being located on one of said fin connectors as a region of stressor material filling in an interior portion of said fin connector.

2. (Rejected) The method of claim 1, wherein said at least one localized stressor region comprises a first localized stressor region, said method further comprising:

forming a second localized stressor region within said device,

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed.

3. (Rejected) The method of claim 2, wherein said first localized stressor region and said second localized stressor region comprise a same type material.

4. (Rejected) The method of claim 3, wherein said same type material comprises one of a compressive stressor material and a tensile stressor material.

5. (Canceled)

6. (Rejected) The method of claim 2, wherein said first and second localized stressor regions are formed on said fin connectors of said FinFET as regions of stressor material filling in interior portions of respective two fin connectors.

7-9. (Canceled)

10. (Rejected) The method of claim 4, wherein said same type material comprises a compressive material and primary charge carriers in said region being stressed comprise holes.

11. (Rejected) The method of claim 4, wherein said same type material comprises a tensile material and primary charge carriers in said region being stressed comprise electrons.

12. (Rejected) The method of claim 2, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress.

13. (Rejected) The method of claim 1, wherein said device comprises one of a plurality of devices in an electronic circuit, said method further comprising:

selectively providing a blocking mask over devices in said electronic circuit which are not to receive said at least one localized stressor region.

14. (Rejected) A method of forming a stress region in an electronic device, said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors, said method comprising:

forming a first localized stressor region within said device on a first fin connector as comprising a first region of stressor material filling in an interior portion of said first fin connector; and

forming a second localized stressor region within said device on a second fin connector as comprising a second region of stressor material filling in an interior portion of said second fin connector,

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed.

15. (Rejected) The method of claim 14, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress.

16-22. (Canceled)

23. (Rejected) The method of claim 1, wherein at least one of said at least one localized stressor region interacts with a stressed region located outside said device.

24. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to generate one of a compression stress and a tensile stress.

25. (Rejected) The method of claim 1, wherein said at least one localized stressor region is located within said device to generate a stress that enhances a performance of said device.

26. (Rejected) The method of claim 25, wherein said performance enhancement comprises an increase in a carrier mobility.

27. (Rejected) The method of claim 25, wherein said performance enhancement comprises a decrease in a carrier mobility.

28. (Rejected) The method of claim 1, wherein said at least one localized stressor region is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow.

29. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to create a symmetrically stressed region.

30. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to create an asymmetrically stressed region.

IX. EVIDENCE APPENDIX

(NONE)

X. RELATED PROCEEDINGS APPENDIX

(NONE)